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ASYMPTOTIC ANALYSIS OF PHASE CONTROL SYSTEM FOR CLOCKS IN MULTIPROCESSOR ARRAYS

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Abstract: New method for the rigorous mathematical analysis of electronic synchronization systems is suggested. This method allows to calculate the characteristics of phase detectors and carry out a rigorous mathematical analysis of transient process and stability of the system.

1 INTRODUCTION

In recent years, it has actively produced and used array processors systems, which face the problem of generation of synchronous signals and the mutual synchronization of processors.

In realizing parallel algorithms, the processors must perform a certain sequence of operations simultaneously. These operations are to be started at the moments of arrival of clock pulses at processors. Since the paths along which the pulses run from the clock to every processor are of different length, a mistiming in the work of processors arises. This phenomenon is called a clock skew.

The elimination of the clock skew is one of the most important problems in parallel computing and information processing (as well as in the design of array processors).

Several approaches to solving the problem of eliminating the clock skew have been devised for the last thirty years.

In developing the design of multiprocessor systems, a way was suggested Kung, 1988 for joining the processors in the form of an H-tree, in which (Fig. 1) the lengths of the paths from the clock to every processor are the same. However, in this case the clock skew is not eliminated completely because of heterogeneity of the wires (Kung, 1988). Moreover, for a great number of processors, the configuration of communication wires is very complicated. This leads to difficult technological problems.

Among the disadvantages we note the deceleration of performance of parallel algorithms. In addition to the problem of eliminating the clock skew, another important problem arose. The increase in the number of processors in multiprocessor systems required an increase in the power of the clock. But the powerful clock came to produce significant electromagnetic noise. Not so long ago a new method for eliminating the clock skew and reducing the generator's power was suggested. It consists of introducing a special distributed system of clocks controlled by phase-locked loops (Fig. 2). This approach enables one to reduce significantly the power of clocks.

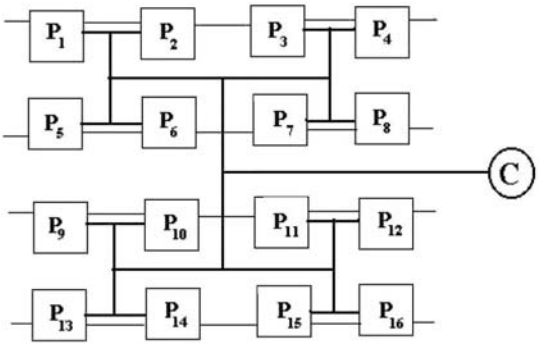

Figure 1: H-tree.

Phase-locked loops (PLLs) are widely used in telecommunication and computer architectures. They were invented in the 1930s-1940s (De Bellescize, 1932; Wendt & Fredentall, 1943) and then the theory and practice of PLLs were intensively studied (Viterbi, 1966; Lindsey, 1972; Gardner, 1979).