ICINCO 2009 - 6th International Conference on Informatics in Control, Automation and Robotics, Proceedings, Volume 3 SPSMC, 2009, pp. 221-224
(doi: 10.5220/0002205002210224)

ANALYSIS AND DESIGN OF COMPUTER ARCHITECTURE CIRCUITS WITH CONTROLLABLE DELAY LINE

N.V. Kuznetsov, G.A. Leonov, S.M. Seledzhi
Saint-Petersburg State University, Universitetski pr. 28, Saint-Petersburg, 198504, Russia
leonov@math.spbu.ru

P. Neittaanmäki
University of Jyväskylä, P.O. Box 35 (Agora), FIN-40014, Finland
pn@mit.jyu.fi

Keywords: delay line, phase locked loop, nonlinear analysis, clocked circuit

Abstract: In this work classical and modern control theory methods are applied for rigorous mathematical analysis and design of different computer architecture circuits such as clock generators, synchronization systems and others. The present work is devoted to the questions of analysis and synthesis of feedback systems, in which there are controllable delay lines. In the work it is mathematically strictly shown that *RC*-chain can be used as a controllable delay line for different problems of circuit engineering if the chain is sequentially connected with hysteretic relay. This relay is either artificially introduced or shows itself as non-ideality of logic elements. The possibility of phase-locked loop application for time delay control is considered.

1 INTRODUCTION

The work is devoted to the questions of analysis and synthesis of feedback systems, in which there are controllable delay lines. First of all this is a class of controllable clock generators and clocked circuits, which perform the functions of summators [Cormen et al., 1990].

In clocked circuits it is necessary that the delay was by the one tact. For this purpose we need in a special setting of parameters of delay lines, which will be described in details. The generators, constructed on logic elements and delay lines, are not high-stable with respect to frequency [Ugrumov, 2000]. Therefore, for their stabilization and synchronization by phase-locked loops it is necessary to introduce a controllable parameter in delay line. A class of such delay lines, the block-scheme of which is shown in Fig. 1, is considered.

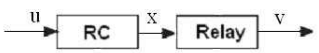

Figure 1: Delay line.

The *RC*-chains are often used in circuit engineering as delay lines [Ugrumov, 2000]. We assume that the relation between the input u and the output x is described by the following standard equation of *RC*-chain

$$RC\frac{dx}{dt} + x = u(t), \qquad (1)$$

where R is a resistance, C is a circuit capacitance.

The relation between the input x and the output v is described by the graph of "relay with hysteresis" function, which is shown in Fig. 2. Here

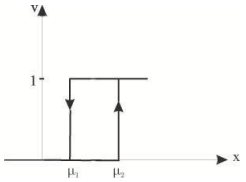

Figure 2: Relay with hysteresis.

μ_1 and μ_2 are certain numbers from the interval $(0, 1)$. The theory and practice of application of such relay blocks in feedback systems is well described in [Popov, 1979; Krasnosel'skii and Pokrovskii, 1983].